REMARKS

This Amendment responds to the Office Action mailed March 27, 2006, in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-30 were previously pending in the application. By this amendment, claims 1, 5, 11, 17 and 22 are amended. Claims 4, 9, 10, 16, 20 and 21 are cancelled without prejudice or disclaimer. Accordingly, claims 1-3, 5-8, 11-15, 17-19 and 22-30 are currently pending, with claims 1 and 17 being independent claims. No new matter has been added.

The Examiner has objected to the title as not descriptive. The title has been amended to be more descriptive. Accordingly, withdrawal of the objection to the title is respectfully requested.

The Examiner has objected to the drawings because formal drawings have not yet been submitted. Enclosed herewith are formal drawings for replacement of the drawings as filed. Accordingly, withdrawal of the drawing objection is respectfully requested.

The Examiner has objected to claims 1 and 17 because of various informalities. The amended claims incorporate the corrections suggested by the Examiner. Accordingly, withdrawal of the claim objections is respectfully requested.

The Examiner has rejected claims 1-30 under 35 U.S.C. §102(b) as anticipated by Parthasarathy (US 6,671,799). The rejection is respectfully traversed in view of the amended claims.

Parthasarathy discloses a system and method for dynamically sizing hardware loops and executing nested loops in a digital signal processor. The disclosed apparatus includes N pairs of loop start registers and loop end registers, each loop start register storing a loop start address and each loop end register storing a loop end address, and N comparators, each of the N comparators associated with one of the N pairs of loop start registers and loop end registers.

Each of the N comparators compares a selected one of a first loop start address and a first loop end address to a fetch program counter value to detect one of a loop start hit and a loop end hit (col. 2, lines 14-25). The loop start/end detection circuit is shown in FIG. 3 of Parthasarathy. Output results of comparators 321-323 are provided to priority match circuitry 305, which resolves instances of multiple hits according to the convention that loops are always fully nested (col. 7, lines 31-38).

Amended claim 1 is directed to a method for issuing instructions and a processor having a pipeline and requires, in part, providing a loop buffer for holding program loop instructions and a register file having at least three entries for holding speculative and architectural loop control parameters, wherein each entry in the register file comprises a loop top register for holding a loop top address, a loop bottom register for holding a loop bottom address and a loop count register for holding a loop count, selecting the loop top address of the current entry from the loop top addresses in the register file, comparing, in a single loop top comparator, a current instruction address with the selected loop top address to determine a loop top match, selecting the loop bottom address of the current entry from the loop bottom addresses in the register file, and comparing, in a single loop bottom comparator, the current instruction address with a selected loop bottom address to determine a loop bottom match.

Parthasarathy does not disclose or suggest *selecting the loop top address of the current entry from the loop top addresses* in the register file, *comparing, in a single loop top comparator*, a current instruction address with the selected loop top address, *selecting the loop bottom address of the current entry from the loop bottom addresses* in the register file, and *comparing, in a single loop bottom comparator*, the current instruction address with the selected loop bottom address, as required by amended claim 1. Parthasarathy does not disclose the concept of a current entry in the register file or of selecting the parameters of the current entry. Instead, Parthasarathy compares the loop top or loop bottom for all of the loops to a fetch program counter, as shown in FIG. 3. This operation is necessary because Parthasarathy operates "according to the convention that loops are always fully nested" (col. 7, lines 37-38). In accordance with the teachings of the present invention, nested program loops can be handled by

providing two loop buffers, each with a register file as shown in FIG. 3 (page 8, lines 21-25 of the specification). Parthasarathy does not disclose or suggest the above limitations of amended claim 1. Accordingly, amended claim 1 is clearly and patentably distinguished over Parthasarathy, and withdrawal of the rejection is respectfully requested.

Claims 2, 3, 5-8 and 11-15 depend from claim 1 and are patentable over Parthasarathy for at least the same reasons as amended claim 1.

Amended claim 17 is directed to apparatus for issuing instructions in a processor having a pipeline and requires, in part, a loop buffer for holding program loop instructions, a register file having at least three entries for holding speculative and architectural loop control parameters, a loop top selector for selecting the loop top address of the current entry from the loop top addresses in the register file, a single loop top comparator for comparing a current instruction address with the selected loop top address to determine a loop top match, a loop bottom selector for selecting the loop bottom address of the current entry from the loop bottom addresses in the register file, and a single loop bottom comparator for comparing the current instruction address with the selected loop bottom address to determine a loop bottom match.

As discussed above in connection with claim 1, Parthasarathy does not disclose or suggest a loop top selector for selecting the loop top address of the current entry from the loop top addresses in the register file, a single loop top comparator for comparing a current instruction address with the selected loop top address, a loop bottom selector for selecting the loop bottom address of the current entry from the loop bottom addresses in the register file, and a single loop bottom comparator for comparing the current instruction address with the selected loop bottom address. Parthasarathy contains no disclosure of a current entry in the register file or of selecting the parameters of the current entry. Instead, Parthasarathy discloses comparators for comparing the loop top or loop bottom for all of the loops to the fetch program counter. For these reasons and for the reasons discussed above in connection with claim 1, amended claim 17 is clearly and patentably distinguished over Parthasarathy. Accordingly, withdrawal of the rejection is respectfully requested.

Claims 18, 19 and 22-30 depend from claim 17 and are patentable over Parthasarathy for at least the same reasons as claims 1 and 17.

Based upon the above discussion, claims 1-3, 5-8, 11-15, 17-19 and 22-30 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests the necessary two month extension of time. If the fee occasioned by this response is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Dated: August 23, 2006
X08/27/06

Respectfully submitted,

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